WHAT IS CLAIMED IS:

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1. A variable gain amplifier comprising:

a first amplification stage; and

a second amplification stage in communication with said first amplification stage, wherein a high frequency response of said amplifier is maintained by selectively varying an adjustable capacitor disposed on said second amplification stage.

2. The amplifier of claim 1 wherein a gain of said amplifier comprises a combination of a first stage gain and a second stage gain:

wherein said first amplification stage comprises a first transistor network, wherein said first stage gain is varied by varying resistance in a circuit path of said first transistor network; and

wherein said second amplification stage comprises a second transistor network, wherein said second stage gain is varied by varying resistance in a circuit path of said second transistor network.

3. The amplifier of claim 2 wherein said first and second transistor networks comprise differential pairs of transistors.

4. The amplifier of claim 3 wherein said adjustable capacitor is adjusted responsive to varying said gain of said amplifier.

5. The amplifier of claim 2 constructed substantially on a single integrated circuit substrate.

6. The amplifier of claim 3 constructed substantially on a single integrated circuit substrate.

7. A method for maintaining a high frequency response of a variable gain amplifier comprising the steps of:

selectively varying a gain of said amplifier; and

adjusting a variable capacitor responsive to said selectively varying said gain step, wherein said high frequency response of said amplifier remains substantially constant.

8. The method of claim 7 wherein said amplifier comprises a multistage amplifier having at least a first and a second amplification stage, wherein said selectively varying said gain step comprises the steps of:

selectively varying a gain of said first amplification stage; and

selectively varying a gain of said second amplification stage.

9. The method of claim 8, wherein said variable capacitor is disposed on said second amplification stage.

10. The method of claim 7 performed substantially on single integrated circuit substrate.

11. The method of claim 9 performed substantially on a single integrated circuit substrate.

12. A variable gain amplifier comprising:

a first amplification stage; and

a second amplification stage in communication with said first amplification stage, wherein said first amplification stage and said second amplification stage are adapted to cooperate such that a first mode of operation provides gain adjustment of an input signal while substantially maintaining a Third-Order Output Intercept Point (OIP3) and a second mode of operation provides gain adjustment of said input signal while substantially maintaining a Third-Order Input Intercept Point (IIP3).

13. The amplifier of claim 12 wherein said amplifier is adapted to receive a first class of inputs needing a substantially constant OIP3 and a second class of inputs needing a substantially constant IIP3.

14. The amplifier of claim 13 wherein said first class of inputs comprise cable frequency channels and said second class of inputs comprise broadcast frequency channels.

15. The amplifier of claim 13 further comprising:

a variable first stage gain; and

a variable second stage gain, wherein adjusting said variable first stage gain while maintaining said variable second stage gain results in substantially maintaining said OIP3, and wherein adjusting said variable second stage gain while maintaining said variable first stage gain results in substantially maintaining said IIP3, and wherein said adjusting said variable first stage gain substantially maintains a high frequency response of said amplifier.

16. The amplifier of claim 15:

wherein said first amplification stage comprises a first amplifier, wherein said variable first stage gain is controlled by a first stage resistor and a first stage variable resistor network; and

wherein said second amplification stage comprises a second amplifier, wherein said variable second stage gain is controlled by a second stage resistor, a second stage variable resistor network, and a second stage variable capacitor network.

17. The amplifier of claim 16 wherein said first and second stage variable resistor networks each comprise a plurality of resistors in communication with a plurality of resistor associated transistors, wherein resistance of said first or second amplification stage is controlled by selectively and sequentially varying the effective resistance of said resistor associated transistors.

18. The amplifier of claim 17 wherein said second stage variable capacitor network comprises a plurality of capacitors in communication with a plurality of capacitor associated transistors, wherein impedance of said second amplification stage is controlled by selectively and sequentially varying the effective resistance of said capacitor associated transistors.

19. The amplifier of claim 18 wherein said effective resistance of said transistors is varied by adjusting the biasing of said transistors.

20. The amplifier of claim 18 wherein varying said variable first stage resistor network varies said variable second stage capacitor network such that capacitance increases as resistance decreases and capacitance decreases as resistance increases.

21. The amplifier of claim 20 wherein said decrease of resistance in said variable first stage resistor network reduces a bandwidth of said first stage.

22. The amplifier of claim 21 wherein said increase of capacitance of said variable second stage capacitor network responsive to said decrease in resistance of said variable first stage resistor network increases a bandwidth of said amplifier.

23. The amplifier of claim 12 constructed substantially on a single integrated circuit substrate.

24. The amplifier of claim 18 constructed substantially on a single integrated circuit substrate.

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25. A method for providing variable gain amplification comprising the steps of:

selecting an operating mode of a plurality of operating modes of an amplifier based at least in part on an input signal characteristic; and

varying a gain of said amplifier based at least in part on said selected operating mode.

26. The method of claim 25, wherein said selected operating mode of said amplifier maintains a particular Third-Order Intercept Point (IP3).

27. The method of claim 26, wherein said amplifier comprises a plurality of amplification stages, each of said amplification stages having a variable gain contribution to a total gain of said amplifier, and wherein said varying said gain step comprises the steps of:

selecting a particular amplification stage for manipulation based at least in part on said selected operating mode; and

varying a gain of said selected amplification stage.

28. The method of claim 27 wherein said input signal characteristic suggests maintaining a substantially constant output IP3 (OIP3) when said input signal is amplified.

29. The method of claim 28 wherein said selected amplification stage is a first stage, wherein said selected operating mode is a first operating mode, and wherein said varying said gain of said selected amplification stage step is controlled by a first stage variable resistor network.

30. The method of claim 29 wherein said first stage variable resistor network comprises a plurality of resistors in communication with a plurality of resistor related transistors, said method further including the step of:

varying biasing conditions of said plurality of resistor related transistors selectively and sequentially, for controlling an effective resistance of said resistor related transistors.

31. The method of claim 30 wherein a high frequency response of said amplifier is maintained by a second stage variable capacitor network variable in response to said varying said biasing conditions of said plurality of resistor related transistors.

32. The method of claim 31 wherein said second stage variable capacitor network comprises a plurality of capacitors in communication with a plurality of capacitor associated transistors, wherein biasing conditions of said capacitor associated transistors are responsively controlled by said biasing conditions of said plurality of resistor related transistors.

33. The method of claim 27 wherein said input signal characteristic suggests maintaining a substantially constant input IP3 (IIP3) when said input signal is amplified.

34. The method of claim 33 wherein said selected amplification stage is a second stage, wherein said selected operating mode is a second operating mode, and wherein said varying said gain of said selected amplification stage step is controlled by a second stage variable resistor network.

35. The method of claim 34 wherein said second stage variable resistor network comprises a plurality of resistors in communication with a plurality of resistor associated transistors, said method further including the step of:

varying biasing conditions of said plurality of resistor associated transistors selectively and sequentially for controlling an effective resistance of each of said resistor associated transistors.

36. A variable gain amplifier comprising:

a first stage comprising:

a first stage transistor;

a load resistor connected to said first stage transistor; and

a adjustable first stage resistor connected to said first stage transistor; and

a second stage comprising:

a second stage transistor, wherein an input to said second stage transistor is connected to an output of said first transistor;

an adjustable load resistor connected to said second stage transistor;

a second stage resistor connected to said second stage transistor; and

an adjustable capacitor connected in parallel with said second stage resistor for controlling a high frequency response of said amplifier;

wherein a current flow through said first stage and second stage transistors is adjusted to vary the gain of said amplifier, while selectively maintaining a Third-Order Intercept Point (IP3) at a constant level.

37. The invention of claim 36:

wherein said first stage further comprises:

a second transistor, wherein said first stage transistor and said second transistor form a first pair of transistors;

a second load resistor, wherein said load resistor and said second load resistor form a pair of load resistors connected to said first pair of transistors; and

a second adjustable first stage resistor, wherein said adjustable first stage resistor and said second adjustable first stage resistor form a pair of adjustable first stage resistors connected to a common terminal of said first pair of transistors; and

wherein said second stage further comprises:

a second transistor, wherein said second stage transistor and said second transistor form a second pair of transistors, wherein an input of said second transistor is connected to an output of said second transistor of said first stage;

a second adjustable load capacitor, wherein said adjustable load capacitor and said second adjustable load capacitor form a pair of adjustable load capacitors connected to said second pair of transistors; and

a second resistor, wherein said second stage resistor and said second resistor form a pair of second stage resistors connected to a common terminal of said second pair of transistors, wherein said adjustable capacitor is connected in parallel with said pair of second stage resistors.

38. The invention of claim 37 wherein said current flow is adjusted by selectively varying said adjustable resistors of said first stage, said adjustable load resistors of said second stage, and said adjustable capacitor of said second stage.

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39. The invention of claim 38 wherein said adjustable resistors of said first stage and said adjustable load resistors of said second stage each comprise a network having a plurality of resistors connected to a plurality of resistor associated transistors, wherein a resistance of a circuit path of said amplifier is controlled by selectively and sequentially varying biasing conditions for said resistor associated transistors to control an effective resistance of said resistor associated transistors.

40. The invention of claim 39 wherein said adjustable capacitor of said second stage comprises a network having a plurality of capacitors connected to a plurality of capacitor associated transistors, wherein a capacitance of a circuit path of said amplifier is controlled by selectively and sequentially varying biasing conditions for said capacitor associated transistors to control an effective resistance of said capacitor associated transistors, wherein said capacitance is added in proportion to a current allowed by said effective resistance of said capacitor associated transistors.

41. The invention of claim 40 wherein input signals require selectively maintaining an Input IP3 (IIP3) constant.

42. The invention of claim 41 wherein said input signals comprise broadcast frequency signals which require a high input linearity.

43. The invention of claim 40 wherein input signals require selectively maintaining an Output IP3 (OIP3) constant.

44. The invention of claim 43 wherein said input signals comprise cable frequency signals which require a high output linearity.

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45. The invention of claim 41 wherein said first and second pairs of transistors are bipolar transistors and wherein said IIP3 is held constant by maintaining a pair of adjustable emitter resistors of said first stage constant while selectively and sequentially varying a pair of adjustable collector resistors of said second stage.

46. The invention of claim 41 wherein said first and second pairs of transistors are field effect transistors (FET) and wherein said IIP3 is held constant by maintaining a pair of adjustable source resistors of said first stage constant while selectively and sequentially varying a pair of adjustable drain resistors of said second stage.

47. The invention of claim 43 wherein said first and second pairs of transistors are bipolar transistors and wherein said OIP3 is held constant by maintaining a pair of adjustable collector resistors of said second stage constant while selectively and sequentially varying a pair of adjustable emitter resistors of said first stage.

48. The invention of claim 43 wherein said first and second pairs of transistors are FETs and wherein said OIP3 is held constant by maintaining a pair of adjustable drain resistors of said second stage constant while selectively and sequentially varying a pair of adjustable source resistors of said first stage.

49. The invention of claim 40 wherein said adjustable capacitor and said adjustable first stage resistors are controlled by identical biasing conditions configured to simultaneously increase capacitance as first stage resistance decreases and to simultaneously decrease capacitance as first stage resistance increases.

50. The invention of claim 36 further comprising:

a third stage comprising:

a third transistor, wherein an input of said third transistor is connected to an output of said second transistors;

a variable capacitor connected between said output of said second stage and said input of said third stage; and

a variable resistor connected between said output of said second stage and said input of said third stage.

51. The invention of claim 50:

wherein said third stage further comprises:

a second transistor, wherein said third transistor and said second transistor form a third pair of transistors;

a second variable capacitor, wherein said variable capacitor and said second variable capacitor form a pair of variable capacitors connected between said outputs of said second stage and inputs of said third stage; and

a second variable resistor, wherein said variable resistor and said second variable resistor form a pair of variable resistors connected between said outputs of said second stage and said inputs of said third stage.

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52. The invention of claim 51 wherein said pair of variable capacitors each comprise a network having a plurality of capacitors connected to a plurality of capacitor affiliated transistors, wherein capacitance of a circuit path of said amplifier is controlled by selectively and sequentially varying biasing conditions for said capacitor affiliated transistors to control an effective resistance of said capacitor affiliated transistors, wherein said capacitance is added in proportion to a current allowed by said effective resistance of said capacitor affiliated transistors.

53. The invention of claim 52 wherein said pair of variable resistors each comprise a network having a plurality of resistors connected to a plurality of resistor affiliated transistors, wherein resistance of a circuit path of said amplifier is controlled by selectively and sequentially varying biasing conditions for said resistor affiliated transistors to control an effective resistance of said resistor affiliated transistors.

54. The invention of claim 51 wherein said third pair of transistors are bipolar transistors.

55. The invention of claim 51 wherein said third pair of transistors are FETs.

56. The invention of claim 53 wherein said pair of variable capacitors and said pair of variable resistors are configured as a high pass filter to selectively control said high frequency response.

57. The invention of claim 56 wherein said pair of variable capacitors and said pair of variable resistors are varied so as to selectively control a center frequency of said high pass filter, wherein said selected center frequency encompasses a signal of interest.

58. The invention of claim 37 constructed substantially on a single integrated circuit substrate.

59. The invention of claim 39 constructed substantially on a single integrated circuit substrate.

60. The invention of claim 40 constructed substantially on a single integrated circuit substrate.

61. The invention of claim 56 constructed substantially on a single integrated circuit substrate.

62. The invention of claim 53 constructed substantially on a single integrated circuit substrate.

63. A method of adjusting a gain of a variable gain amplifier, wherein said amplifier includes at least two stages, said method comprising the steps of:

adjusting a pair of variable common resistors of a first stage and a pair of variable load resistors of a second stage to selectively vary said gain while maintaining a constant Third-Order Intercept Point (IP3);

changing a variable capacitance in order to selectively vary a high frequency cut-off point to adjust said bandwidth; and

modifying biasing conditions for each of said transistor pairs responsive to a varying amplifier current.

64. The method of claim 63 wherein said variable common resistors and said variable load resistors each comprise a network having a plurality of resistors connected to a plurality of associated transistors, said adjusting step comprising the step of:

selectively and sequentially controlling operating conditions for each of said associated transistors in order to vary an effective resistance of said associated transistors.

65. The method of claim 64 wherein input signals require maintaining a constant input IP3 (IIP3).

66. The method of claim 64 wherein input signals require maintaining a constant output IP3 (OIP3).

67. The method of claim 65 wherein each of said transistor pairs comprises bipolar transistors, said adjusting step further comprising the steps of:

maintaining a pair of variable emitter resistors of said first stage at a constant value; and

adjusting a pair of variable collector resistors of said second stage.

68. The method of claim 66 wherein each of said transistor pairs comprises bipolar transistors, said adjusting step further comprising the steps of:

maintaining a pair of variable collector resistors of said second stage at a constant value; and

adjusting a pair of variable emitter resistors of said first stage.

69. The method of claim 65 wherein each of said transistor pairs comprises field effect transistors (FET), said adjusting step further comprising the steps of:

maintaining a pair of variable source resistors of said first stage at a constant value; and

adjusting a pair of variable drain resistors of said second stage.

70. The method of claim 66 wherein each of said transistor pairs comprises FETs and, said adjusting step further comprising the steps of:

maintaining a pair of variable drain resistors of said second stage at a constant value; and

adjusting a pair of variable source resistors of said first stage.

71. The method of claim 63 wherein said variable capacitance comprises networks having a plurality of capacitors connected to a plurality of capacitance associated transistors, said changing step comprising the step of:

selectively and sequentially controlling the operating conditions of said capacitance associated transistors so as to vary an effective resistance of said capacitance associated transistors, wherein said capacitance is changed in proportion to a current controlled by said effective resistance.

72. The method of claim 64 wherein said variable capacitance and said variable common resistors are controlled by identical operating conditions configured to increase capacitance in unison with decreasing common resistance and to decrease capacitance in unison with increasing common resistance.

73. The method of claim 63 further comprising the steps of:

filtering outputs of said second stage in a third stage to further adjust said bandwidth; and

buffering said outputs through a pair of transistors in said third stage, wherein said filtering step is performed by a pair of adjustable capacitors of said third stage connected to a pair of adjustable resistors of said third stage.

74. The method of claim 73 further comprising the steps of:

selectively and sequentially varying said adjustable capacitors of said third stage; and

selectively and sequentially varying said adjustable resistors of said third stage in order to control said bandwidth.

75. The method of claim 74 wherein said adjustable capacitors of said third stage each comprise a network having a plurality of capacitors connected to a plurality of capacitor corresponding transistors, said filtering step further comprising the step of:

selectively and sequentially controlling operating conditions of said capacitor corresponding transistors so as to vary an effective resistance of said capacitor corresponding transistors, wherein said capacitance is changed in proportion to a current controlled by said effective resistance.

76. The method of claim 75 wherein said adjustable resistors of said third stage each comprise a network having a plurality of resistors connected to a plurality of resistor corresponding transistors, said filtering step further comprising the step of:

selectively and sequentially controlling operating conditions of said resistor corresponding transistors so as to vary an effective resistance of said resistor corresponding transistors.

77. A variable capacitor comprising:

at least one variable capacitor unit, said capacitor unit comprising:

a capacitor;

at least two transistors each connected in series with said capacitor; and

a biasing circuit for biasing said transistors, wherein an impedance value of said capacitor unit is controlled by selectively varying said biasing for said transistors to control an effective resistance of said transistors, wherein said impedance is varied in proportion to a current allowed by said effective resistance of said transistors.

78. The variable capacitor of claim 77 wherein each of said capacitor units are connected to each other in parallel.

79. The variable capacitor of claim 77 wherein said variable capacitor is adjusted across a total impedance range by sequentially varying between a minimum and maximum impedance value of each of said variable capacitor units.

80. The variable capacitor of claim 77 wherein said transistors are field effect transistors (FET).